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APPLICATION FOR LETTERS PATENT

Methods of Forming Semiconductor Stacked Die Devices

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RELATED APPLICATION

This application is a divisional application of and claims priority to U.S. Patent Application Serial No. 09/679,143, filed on October 3, 2000, the disclosure of which is incorporated by reference herein.

TECHNICAL FIELD

This invention relates to generally to method of forming semiconductor devices and, more particularly to method of forming semiconductor stacked die constructions.

BACKGROUND

Semiconductor devices are typically constructed from a silicon or gallium arsenide wafer through a process involving a number of deposition, masking, diffusion, etching, and implanting steps. Usually, many individual devices are constructed on the same wafer. After fabrication, the wafer is typically sawed or otherwise singulated into individual units, where each unit takes the form of an integrated circuit (IC) die.

It has become a practice in the industry to provided integrated circuit devices in the form of so-called "stacked die" arrangements. Stacked die arrangements typically involve two or more IC die that are fixed upon one another, typically through some type of adhesive arrangement. Interconnections can then be made between the individual die to provide an overall device with a desirable density and enhanced functionality.

Examples of stacked die arrangements are described in detail in the following U.S. Patents, to which the reader is referred for additional detail: U.S.

Patent Nos. 5,291,061; 6,051,886; 5,397,916; 5,434,745; 6,093,939; and 5,864,177.

To date, interconnections between the individual die of stacked die arrangements have been made at or near the periphery of each die. U.S. Patent Nos. 5,291,061, and 5,397,916 provide very good examples of this type of interconnection. As device processing speeds continue to increase, those involved in the design of semiconductor devices are necessarily forced to consider and reconsider traditionally accepted notions of circuit design. One particular area of interest in the industry concerns the design and fabrication of memory devices, and particularly those memory devices that employ stacked die arrangements.

Accordingly, this invention arose out of concerns associated with providing improved systems that employ stacked die arrangements, and methods of forming the same.

SUMMARY

Semiconductor devices and methods of forming semiconductor devices are described. In one embodiment, a method comprises forming at least one conductive structure within a plurality of semiconductor substrates, said act of forming comprising first forming said at least one conductive structure to extend into a respective semiconductor substrate a distance that is less than an elevational thickness of the substrate, and second removing substrate material elevationally adjacent said one conductive structure effective to expose a surface of said one conductive structure, at least portions of one of the conductive structures having oppositely facing, exposed outer surfaces; and stacking individual substrates

together such that individual conductive structures on each substrate are in electrical contact with the conductive structures on a next adjacent substrate.

In another embodiment, a method comprises forming at least one conductive structure within each of a plurality of semiconductor substrates, said at least one conductive structure comprising a multi-layered structure formed through successive depositions and etchings and having oppositely-facing surfaces; exposing portions of each oppositely-facing surface on at least one of the substrates; and processing the substrates sufficient to form electrical connections between the substrates, said processing comprising stacking the substrates on one another so that the conductive structures on adjacent substrates are electrically connected.

In another embodiment, a method comprises forming at least one conductive structure within each of a plurality of semiconductor substrates, each conductive structure having oppositely-facing surfaces; after said forming, exposing portions of at least one oppositely-facing surface on at least one of the substrates, said exposing comprising etching portions of said at least one substrate to expose said at least one surface; and processing the substrates sufficient to form electrical connections between the substrates by stacking the substrates on one another so that electrical connection can be made between conductive structures on adjacent substrates, said processing comprising: forming additional conductive material over and in electrical contact with said exposed portions; and bonding at least some of the additional conductive material on one substrate with additional conductive material on another of the substrates.

In a further embodiment, a method comprises forming at least one multi-layered, conductive pad structure within each of a plurality of semiconductor

substrates, each conductive pad structure having oppositely-facing surfaces; exposing portions of each oppositely-facing surface on at least one of the substrates, at least one oppositely-facing surface being exposed by etching portions of said at least one substrate to expose said at least one surface; and after said exposing, forming additional conductive material over and in electrical contact with said exposed portions by plating more than one additional conductive material over said exposed portions.

In yet another embodiment, a method comprises a step for providing a multi-layered structure within a plurality of substrates, the multi-layered structures having a front side and a back side; a step for thinning at least one of the substrates after providing the multi-layered structure; a step for exposing portions of the back side of said at least one substrate that was thinned; a step for forming additional conductive material over and in electrical contact with the multi-layered structure of the substrate that was thinned; and a step for stacking the substrates such that the multi-layered structures with the substrates are in electrical contact with one another.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic side sectional view of a semiconductor wafer fragment, in process, in accordance with the described embodiment.

Fig. 2 is diagrammatic side sectional view of the Fig. 1 wafer fragment, in process, in accordance with the described embodiment.

Fig. 3 is a diagrammatic side sectional view of the Fig. 2 wafer fragment, in process, in accordance with the described embodiment.

Fig. 4 is a diagrammatic side sectional view of the Fig. 3 wafer fragment, in process, in accordance with the described embodiment.

Fig. 5 is a diagrammatic side sectional view of two exemplary substrates mounted in a stacked die arrangement in accordance with the described embodiment.

Fig. 6 is a diagrammatic side sectional view of four exemplary substrates mounted in a stacked die arrangement in accordance with the described embodiment.

Fig. 7 is a diagrammatic side sectional view of the Fig. 6 wafer fragment, in process, in accordance with the described embodiment.

DETAILED DESCRIPTION

Exemplary Embodiment

Fig. 1 shows a semiconductor wafer, in process, generally at 10 and includes a semiconductor substrate 12. In the context of this document, the term "semiconductor substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon) and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure including, but not limited, to the semiconductive substrates described above.

Substrate 12 includes regions 14 that are fabricated to contain or comprise integrated circuit (IC) devices. In a preferred implementation, the integrated circuit devices comprise memory devices. One type of exemplary memory device

is a dynamic random access memory (DRAM) device, such as DRAM devices designed by the assignee of this document. It is to be understood, however, that this constitutes but one exemplary type of integrated circuit device that can be provided. Other types of integrated circuit devices (and not necessarily memory devices) can be provided without departing from the spirit and scope of the claimed subject matter.

A pair of regions 16 are shown and comprise interface regions that are designed to provide an interface between the integrated circuit devices within regions 14 and other circuitry that is external of the substrate 12.

A conductive structure 18 is formed within and supported by substrate 12. The exemplary structure 18 can comprise any suitable type of conductive structure and is positioned to make electrical contact with regions 16, and other conductive structures that will ultimately electrically connect the integrated circuit devices to the outside world, as will become apparent below. In a preferred implementation, conductive structure 18 comprises a multi-layered pad structure that is fabricated during processing of the devices in regions 14. The pad structure preferably comprises aluminum and can be formed through successive deposition/etching (or removal) steps.

The conductive structure can be formed at any suitable location within the substrate. It is desirable, however, to have the conductive structure formed at a substrate location that is not at the periphery of the substrate. This is because the conductive structure is going to be used to form electrical connections with other similar conductive structures on other substrates. These substrates will be mounted together in a stacked arrangement so that adjacent substrates are electrically connected through the conductive structures. The manner in which

these electrical connections is to be made desirably eliminates the need to make such electrical connections between the substrates at the periphery of, and external to the substrates, as will become apparent below. In the illustrated example, the conductive structure is disposed within the center of the substrate.

An insulative layer 20 is formed over substrate 12 and patterned to expose a front side 18a of conductive structure 18 as shown.

Referring to Fig. 2, wafer 10 is processed to remove a portion of the back side of the wafer, thus thinning the wafer. The wafer can be thinned through the use of any suitable techniques. For example, the wafer can be mechanically (or chemically-mechanical) abraded or polished to achieve the desired thinned wafer.

Referring to Fig. 3, portions of the wafer are removed, as by any suitable processing technique, sufficient to expose at least a portion of backside 18b of conductive structure 18. In the illustrated example, material of the wafer can be selectively etched, relative to the material from which the conductive structure 18 is formed, so that the back side 18b of the conductive structure is exposed. Thus, at this point in the processing of wafer 12, conductive structure 18 has portions of both of its oppositely-facing surfaces exposed.

Referring to Fig. 4, additional conductive material 22, 24 is formed respectively, over and in electrical contact with the oppositely-facing surfaces (i.e. front side 18a and back side 18b) of conductive structure 18. In the illustrated and described embodiment, the conductive material is formed through known plating techniques. In this specific example, more than one conductive material is plated over the conductive structure 18. Specifically, a first conductive material 26, such as nickel, is first formed over the exposed surfaces of the conductive structure 18. Any suitable plating technique, e.g. electroless plating, can be used. After the first

conductive material 26 is plated over the exposed surfaces of the conductive structure 18, a second conductive material 28 is formed over and in electrical contact with first conductive material 26. Any suitable techniques can be used such as sputtering, evaporating, or plating to name a few. In the illustrated and described embodiment, second conductive material 28 comprises gold. The second conductive material can, however, comprise any suitable conductive material. For example, an alloy of tin and gold can be used. For purposes of further discussion, conductive material 22 will be referred to as the "top most" conductive material, and conductive material 24 will be referred to as the bottommost" conductive material.

Notice that bottommost conductive material 24 is received entirely within an opening that is defined by a via that exposes the surface of the backside 18b of conductive structure 18. The reason for this will become apparent below.

It should be understood that while only one exemplary substrate is shown as being processed as described, in the preferred embodiment, multiple substrates are typically processed at one time so that they can be eventually joined or bonded together in a die stack.

Referring to Fig. 5, two exemplary substrates 12, 12a are shown. It will be appreciated that substrate 12a can be identical to or different from substrate 12. Substrates 12 and 12a are first moved into engagement with one another and then processed sufficiently such that a conductive bond forms between the bottommost conductive material of substrate 12 and the top most conductive material of substrate 12a. In one exemplary implementation, the conductive bond can be formed by stacking the substrates, either in wafer form or singulated die form, and then joining the conductive material on each of the substrates through ultrasonic

thermal compression. This is a good technique to use when the top- and bottommost conductive materials comprise gold. Other techniques can, of course, be used, e.g. thermal compression.

The Fig. 5 construction can thus comprise a first die 12 having IC devices thereon and a second die 12a also having IC devices thereon. Die 12, 12a are mounted together in a stacked arrangement such that the conductive structures of each die are in electrical contact with one another. Thus, the necessity for any such electrical contact to be made external of the substrates or die can be eliminated.

The above technique can be used to form any suitable number of individual dies into a stacked die arrangement. For example, Fig. 6 shows an arrangement of multiple stacked die that consists of four separate substrates (12-12c) that are joined together as described above. Notice that substrate 12c does not have both faces of its conductive structure 18 exposed.

Hence, the inventive techniques described above enable multiple substrates or die to be formed into a stacked arrangement, with operative electrical connections between the die being made by virtue of conductive structures that are disposed entirely within internal regions of the die. In one preferred embodiment, the conductive structures are formed so that they are generally disposed in the center of each die. It is to be appreciated, however, that the conductive structures can be formed at any suitable location on or within the individual die. In the illustrated and described embodiment, the collection of conductive structures for each die are disposed along a common line A.

Once the die have been formed into a stacked arrangement as described above, they can further processed into individual packages. For example, Fig. 7

shows the Fig. 6 die stack where an insulative layer 30 has been formed over the die stack. A conductive line 32 is provided and makes contact with conductive material 22 of the uppermost die 12. Multiple conductive pads 34 are provided over layer 30, with exemplary solder balls 36 being received over each of the pads 34. Processing the die stack can now continue using conventional techniques to form an IC package, as will be appreciated and understood by those of skill in the art.

The various stacked die arrangements that can be formed through the inventive techniques described above are advantageous in that the connective distances as between the individual die can be drastically reduced over other constructions where connections are typically made at the periphery of the die. This is particularly advantageous in the field of memory devices, e.g. SDRAMs and the like, where, for performance purposes, it is highly desirable to reduce stub lengths to the shortest possible distances. In addition, the inventive techniques can enable increased package capacity while providing constructions that more easily dissipate heat. These constructions can more easily dissipate heat because the conductive material joining the individual die can act as a funneling mechanism for heat. Additionally, other material layers, e.g. non-conductive joining material can be formed on the die surfaces to provide not only mechanical support, but further assist in heat dissipation. In addition, the constructions that are provided by the inventive techniques can reduce the number of I/O connections per die. Other advantages will be apparent to those of skill in the art.

Although the invention has been described in language specific to structural features and/or methodological steps, it is to be understood that the invention defined in the appended claims is not necessarily limited to the specific features or

steps described. Rather, the specific features and steps are disclosed as preferred forms of implementing the claimed invention.